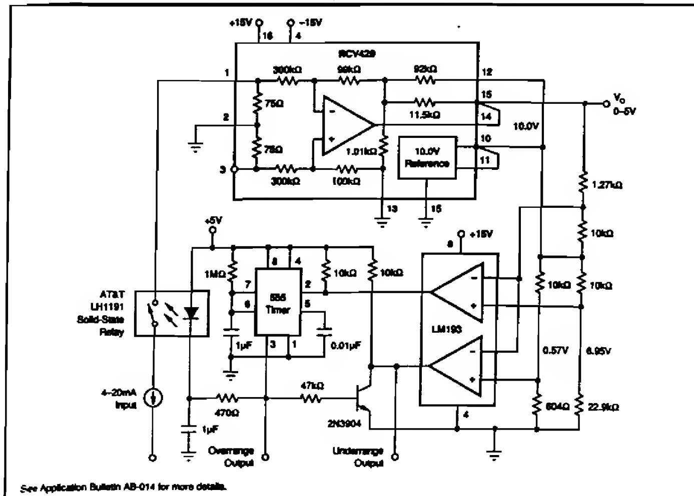

FIGURE 18. 4-20mA Current Loop Receiver with Input Overload Protection.

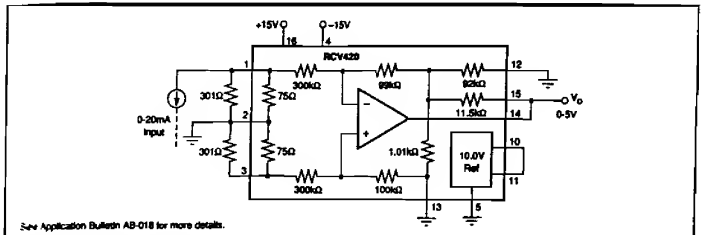

FIGURE 19. 0-20mA/0-5V Receiver Using RCV420.

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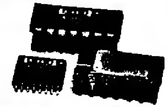


XTR101

AVAILABLE IN DIE

Precision, Low Drift 4-20mA TWO-WIRE TRANSMITTER

FEATURES

- **INSTRUMENTATION AMPLIFIER INPUT**
  Low Offset Voltage, 30µV max
  Low Voltage Drift, 0.75µV/°C max
  Low Nonlinearity, 0.01% max
- **TRUE TWO-WIRE OPERATION**
  Power and Signal on One Wire Pair
  Current Mode Signal Transmission
  High Noise Immunity
- **DUAL MATCHED CURRENT SOURCES**
- **WIDE SUPPLY RANGE, 11.6V to 40V**
- **–40°C to +85°C SPECIFICATION RANGE**
- **SMALL 14-PIN DIP PACKAGE, CERAMIC AND PLASTIC**

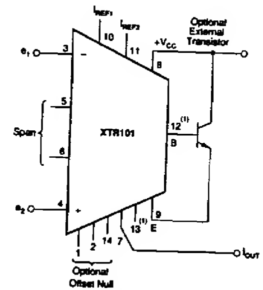
APPLICATIONS

- **INDUSTRIAL PROCESS CONTROL**
  Pressure Transmitters
  Temperature Transmitters
  Millivolt Transmitters
- **RESISTANCE BRIDGE INPUTS**
- **THERMOCOUPLE INPUTS**
- **RTD INPUTS**
- **CURRENT SHUNT (mV) INPUTS**
- **PRECISION DUAL CURRENT SOURCES**
- **AUTOMATED MANUFACTURING**
- **POWER/PLANT ENERGY SYSTEM MONITORING**

DESCRIPTION

The XTR101 is a microcircuit, 4-20mA, two-wire transmitter containing a high accuracy instrumentation amplifier (IA), a voltage-controlled output current source, and dual-matched precision current reference. This combination is ideally suited for remote signal conditioning of a wide variety of transducers such as thermocouples, RTDs, thermistors, and strain gauge bridges. State-of-the-art design and laser-trimming, wide temperature range operation and small size make it very suitable for industrial process control applications. In addition, the optional external transistor allows even higher precision.

The two-wire transmitter allows signal and power to be supplied on a single wire-pair by modulating the power supply current with the input signal source. The transmitter is immune to voltage drops from long runs and noise from motors, relays, actuators, switches, transformers, and industrial equipment. It can be used by OEMs producing transmitter modules or by data acquisition system manufacturers.



NOTE: (1) Pins 12 and 13 are used for optional BW control.

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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-627E

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{CC}$ = 24VDC, R_L = 100Ω with external transistor connected, unless otherwise noted

PARAMETER	CONDITIONS	XTR101AG MIN	XTR101AG TYP	XTR101AG MAX	XTR101BG MIN	XTR101BG TYP	XTR101BG MAX	XTR101AP MIN	XTR101AP TYP	XTR101AP MAX	XTR101AU MIN	XTR101AU TYP	XTR101AU MAX	UNITS
OUTPUT AND LOAD CHARACTERISTICS														
Current	Linear Operating Region	4		20	*		*	*		*	*		*	mA
	Derated Performance	3.8		22	*		*	*		*	*		*	mA
Current Limit			30	38		*	*		31	*		31	*	mA
Offset Current Error	I_{OS}, I_O = 4mA		±3.9	±10		±2.5	±6		±4.5	±19		±4.5	±19	μA
vs Temperature	$\Delta I_{OS}/\Delta T$		±10.5	±20		±8	±15		±10.5	±20		*		ppm, FS°C
Full Scale Output Current Error	Full Scale = 20mA		±30	±80		±15	±60		±60	±80		±60	±80	μA
Power Supply Voltage	V_{CC}, Pins 7 and 8, Compliance(1)	+11.6		+40	*		*	*		*	*		*	VDC
Load Resistance	At V_{CC} = +24V, I_O = 20mA			600			*			600			*	Ω
	At V_{CC} = +40V, I_O = 20mA			1400			*			1400			*	Ω
SPAN														
Output Current Equation	R_S in Ω, e_1 and e_2 in V	I_O = 4mA + [0.016Ω + (40/R_S)] ($e_2 - e_1$)												A/V
Span Equation	R_S in Ω	S = [0.016Ω + (40/R_S)]												
vs Temperature	Excluding TCR of R_S		±50	±100		*	*		*	*		*	*	ppm/°C
Untrimmed Error(2)	ϵ_{span}	−5	−2.5	0	*	*	*	*	*	*	*	*	*	%
Nonlinearity	$\epsilon_{nonlinearity}$			0.01			*			*			*	%
Hysteresis			0			*			*			*		%
Dead Band			0			*			*			*		%
INPUT CHARACTERISTICS														
Impedance: Differential			0.4 ‖ 3			*			*			*		GΩ ‖ pF
Common-Mode			10 ‖ 3			*			*			*		GΩ ‖ pF
Voltage Range, Full Scale	$\Delta e = (e_2 - e_1)$(3)	0		1	*		*	*		*	*		*	V
Offset Voltage	V_{OS}		±30	±60		±20	±50		*	±100		*	±100	μV
vs Temperature	$\Delta V_{OS}/\Delta T$		±0.75	±1.5		±0.35	±0.75		*	*		*	*	μV/°C
Power Supply Rejection	ΔV_{CC}/PSRR = V_{OS} Error	110	125		*	*		*	122		110	122		dB
Bias Current	I_B		80	150		*	*		*	*		*	*	nA
vs Temperature	$\Delta I_B/\Delta T$		0.30	1		*	*		*	*		*	*	nA/°C
Offset Current	I_{OS}		10	±30		*	±20		*	*		*	*	nA
vs Temperature	$\Delta I_{OS}/\Delta T$		0.1	0.3		*	*		*	*		*	*	nA/°C
Common-Mode Rejection(4)	DC	90	100		*	*		*	*		*	*		dB
Common-Mode Range	e_1 and e_2 with Respect to Pin 7	4		6	*		*	*		*	*		*	V
CURRENT SOURCES														
Magnitude			1			*			*			*		mA
Accuracy	V_{CC} = 24V, $V_{PIN 8} - V_{PIN 10, 11}$ = 19V, R_L = 5kΩ, Fig. 5		±0.06	±0.17		±0.025	±0.075		±0.2	±0.37		±0.2	±0.37	%
vs Temperature			±50	±80		±30	±50		*	*		*	*	ppm/°C
vs V_{CC}			±3			*			*			*		ppm/V
vs Time			±8			*			*			*		ppm/month
Compliance Voltage	With Respect to Pin 7	0		V_{CC} − 3.5	*		*	*		*	*		*	V
Ratio Match	Tracking													
Accuracy	$(1 - I_{REF1}/I_{REF2}) \times 100\%$		±0.014	±0.06		±0.009	±0.04		±0.031	±0.088		±0.031	±0.088	%
vs Temperature				±15			10			*			*	ppm/°C
vs V_{CC}			±10			*			*			*		ppm/V
vs Time			±1			*			*			*		ppm/month
Output Impedance		10	20		*	*		*	15		*	15		MΩ
TEMPERATURE RANGE														
Specification		−40		+85	*		*	−40		+85	*		*	°C
Operating		−55		+125	*		*	−40		+85	−40		+85	°C
Storage		−55		+165	*		*	−55		+125	−55		+125	°C

*Same as XTR101AG.

NOTES: (1) See Typical Performance Curves. (2) Span error shown is untrimmed and may be adjusted to zero. (3) e_1 and e_2 are signals on the −In and +In terminals with respect to the output, pin 7. While the maximum permissible Δe is 1V, it is primarily intended for much lower input signal levels, e.g., 10mV or 50mV full scale for the XTR101A and XTR101B grades respectively. 2mV FS is also possible with the B grade, but accuracy will degrade due to possible errors in the low value span resistance and very high amplification of offset, drift, and noise. (4) Offset voltage is trimmed with the application of a 5V common-mode voltage. Thus the associated common-mode error is removed. See Application Information section.

PIN CONFIGURATION

Top View — DIP

1	Zero Adjust	14	Zero Adjust
2	Zero Adjust	13	Bandwidth
3	−In	12	B Control
4	+In	11	I_{REF1}
5	Span	10	I_{REF2}
6	Span	9	E
7	Out	8	$+V_{CC}$

Top View — SOIC (SOL-16 Surface-Mount)

1	Zero Adjust	16	Zero Adjust
2	Zero Adjust	15	Bandwidth
3	−In	14	B Control
4	+In	13	I_{REF1}
5	Span	12	I_{REF2}
6	Span	11	E
7	Out	10	$+V_{CC}$
8	NC	9	NC

DICE INFORMATION

XTR101 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Zero Adjust	8	$+V_{CC}$
2	Zero Adjust	9	E
3	−In	10	I_{REF2}
4	+In	11	I_{REF1}
5	Span	12	B Control
6	Span	13	Bandwidth
7	Out	14	Zero Adjust

NC: No Connection
Substrate Bias: Electrically connected to V− supply.

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	150 x 105 ±5	3.81 x 2.67 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing	Gold	

See "DICE PRODUCTS" Appendix C in Burr-Brown IC Data Book, or contact factory for information.

ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_{CC}$ 40V
Input Voltage, e_1 or e_2 .... $\geq V_{OUT}$, $\leq +V_{CC}$
Storage Temperature Range, Ceramic .... −55°C to +165°C
Plastic .... −55°C to +125°C
Lead Temperature (soldering 10s) G, P .... +300°C
(wave soldering, 3s) U .... +260°C
Output Short-Circuit Duration .... Continuous $+V_{CC}$ to I_{OUT}
Junction Temperature .... +165°C

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
XTR101AG	14-Pin Ceramic DIP	169
XTR101BG	14-Pin Ceramic DIP	169
XTR101AP	14-Pin Plastic DIP	010
XTR101AU	16-Pin SOIC	211

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

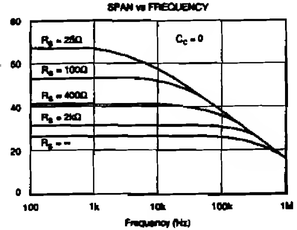
MODEL	PACKAGE	TEMPERATURE RANGE
XTR101AG	14-Pin Ceramic DIP	−40°C to +85°C
XTR101BG	14-Pin Ceramic DIP	−40°C to +85°C
XTR101AP	14-Pin Plastic DIP	−40°C to +85°C
XTR101AU	16-Pin SOIC	−40°C to +85°C
XTR104AD	Dice	−40°C to +85°C

1-24 18.10
75-99 13.65
1103 100's

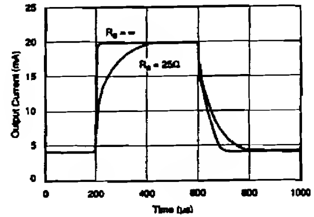
TYPICAL PERFORMANCE CURVES

T_A = +25°C, $+V_{CC}$ = 24VDC unless otherwise noted.

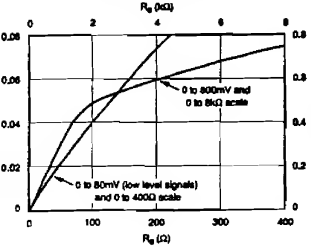
SPAN vs FREQUENCY



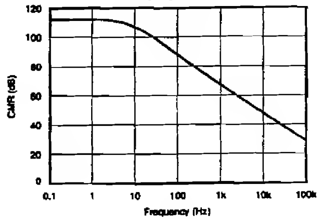
STEP RESPONSE



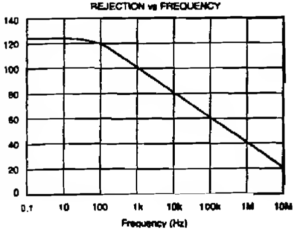
FULL SCALE INPUT VOLTAGE vs R_S



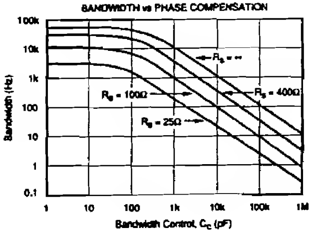
COMMON-MODE REJECTION vs FREQUENCY



POWER SUPPLY REJECTION vs FREQUENCY



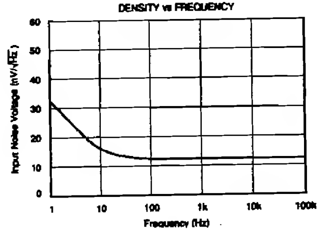
BANDWIDTH vs PHASE COMPENSATION



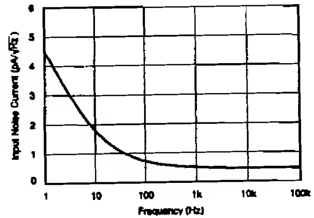
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, $+V_{CC}$ = 24VDC unless otherwise noted.

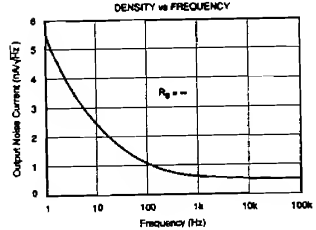
INPUT VOLTAGE NOISE DENSITY vs FREQUENCY



INPUT CURRENT NOISE DENSITY vs FREQUENCY



OUTPUT CURRENT NOISE DENSITY vs FREQUENCY



THEORY OF OPERATION

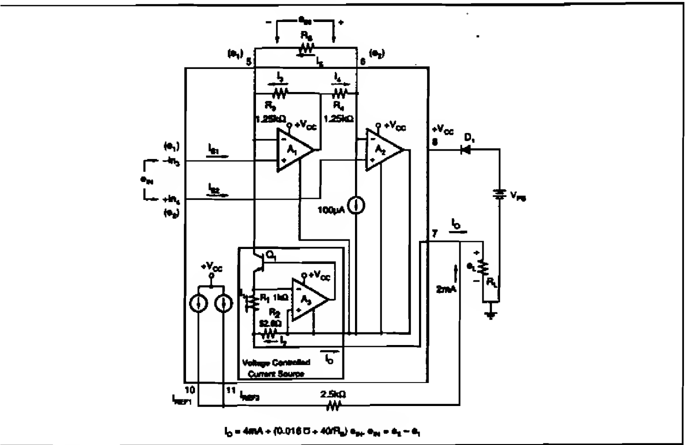
A simplified schematic of the XTR101 is shown in Figure 1. Basically the amplifiers, A_1 and A_2, act as a single power supply instrumentation amplifier controlling a current source, A_3 and Q_1. Operation is determined by an internal feedback loop. e_1 applied to pin 3 will also appear at pin 5 and similarly e_2 will appear at pin 6. Therefore the current in R_S, the span setting resistor, will be $I_S = (e_2 - e_1)/R_S = e_{IN}/R_S$. This current combines with the current, I_3, to form I_1. The circuit is configured such that I_2 is 19 times I_1. From this point the derivation of the transfer function is straightforward but lengthy. The result is shown in Figure 1.

Examination of the transfer function shows that I_O has a lower range-limit of 4mA when $e_{IN} = e_2 - e_1 = 0V$. This 4mA is composed of 2mA quiescent current exiting pin 7 plus 2mA from the current sources. The upper range limit of I_O is set to 20mA by the proper selection of R_S based on the upper range limit of e_{IN}. Specifically R_S is chosen for a 16mA output current span for the given full scale input voltage span; i.e., $(0.016\mho + 40/R_S)(e_{IN}$ full scale) = 16mA. Note that since I_O is unipolar e_2 must be kept larger than e_1; i.e., $e_2 \geq e_1$ or $e_{IN} \geq 0$. Also note that in order not to exceed the output upper range limit of 20mA, e_{IN} must be kept less than 1V when $R_S = \infty$ and proportionately less as R_S is reduced.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR101 is shown in Figure 1. A difference voltage applied between input pins 3 and 4 will cause a current of 4-20mA to circulate in the two-wire output loop (through R_L, V_{PS}, and D_1). For applications requiring moderate accuracy, the XTR101 operates very cost-effectively with just its internal drive transistor. For more demanding applications (high accuracy in high gain) an external NPN transistor can be added in parallel with the internal one. This keeps the heat out of the XTR101 package and minimizes thermal feedback to the input stage. Also in



GURE 1. Simplified Schematic of the XTR101.

ch applications where e_{IN} full scale is small (<50mV) and $_{AN}$ is small (<150Ω), caution should be taken to consider ors from the external span circuit plus high amplification offset drift and noise.

PTIONAL EXTERNAL TRANSISTOR

e optional external transistor, when used, is connected in rallel with the XTR101's internal transistor. The purpose to increase accuracy by reducing heat change inside the TR101 package as the output current spans from 4-20mA. der normal operating conditions, the internal transistor is ver completely turned off as shown in Figure 2. This intains frequency stability with varying external transis- characteristics and wiring capacitance. The actual "cur- n sharing" between internal and external transistors is pendent on two factors: (1) relative geometry of emitter as and (2) relative package dissipation (case size and rmal conductivity). For best results, the external device uld have a larger base-emitter area and smaller package. will, upon turn on, take about [0.95 (I_O – 3.3mA)]mA. wever, it will heat faster and take a greater share after a seconds.

hough any NPN of suitable power rating will operate h the XTR101, two readily available transistors are rec- mended.

2N2222 in the TO-18 package. For power supply volt- ages above 24V, a 750Ω, 1/2W resistor should be con- nected in series with the collector. This will limit the power dissipation to 377mW under the worst-case condi- tions shown in Figure 2. Thus the 2N2222 will safely operate below its 400mW rating at the upper temperature of +85°C. Heat sinking the 2N2222 will result in greatly reduced accuracy improvement and is not recommended.

2. TIP29B in the TO-220 package. This transistor will operate over the specified temperature and output voltage range without a series collector resistor. Heat sinking the TIP29B will result in slightly less accuracy improvement. It can be done, however, when mechanical constraints require it.

ACCURACY WITH AND WITHOUT EXTERNAL TRANSISTOR

The XTR101 has been tested in a circuit using an external transistor. The relative difference in accuracy with and without an external transistor is shown in Figure 3. Notice that a dramatic improvement in offset voltage change with supply voltage is evident for any value of load resistor.

MAJOR POINTS TO CONSIDER WHEN USING THE XTR101

1. The leads to R_S should be kept as short as possible to reduce noise pick-up and parasitic resistance.
2. $+V_{CC}$ should be bypassed with a 0.01µF capacitor as close to the unit as possible (pin 8 to 7).
3. Always keep the input voltages within their range of linear operation, +4V to +6V (e_1 and e_2 measured with respect to pin 7).

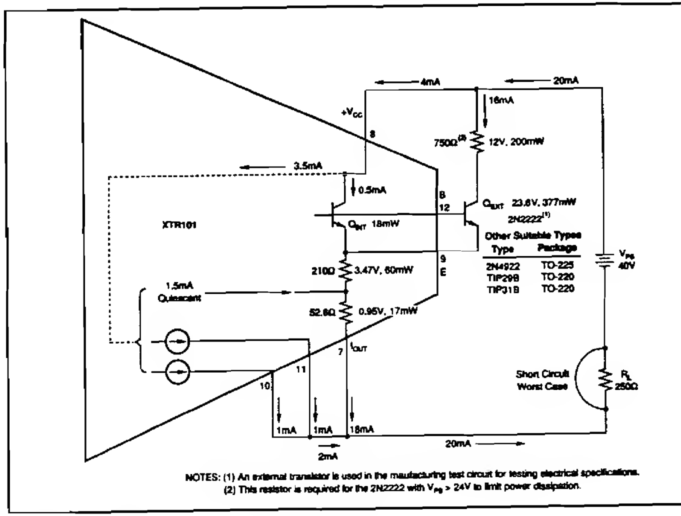


FIGURE 2. Power Calculation of XTR101 with External Transistor.

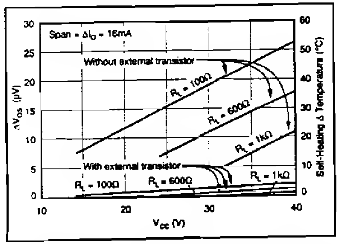


FIGURE 3. Thermal Feedback Due to Change in Output Current.

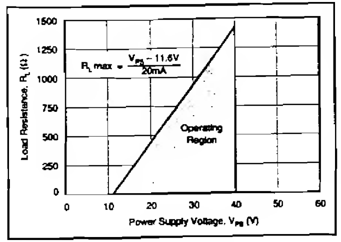


FIGURE 4. Power Supply Operating Range.

4. The maximum input signal level (e_{INFS}) is 1V with $R_S = \infty$ and proportionally less as R_S decreases.
5. Always return the current references (pins 10 and 11) to the output (pin 7) through an appropriate resistor. If the references are not used for biasing or excitation, connect them together to pin 7. Each reference must have between 0V and $+(V_{CC} - 4V)$ with respect to pin 7.
6. Always choose R_L (including line resistance) so that the voltage between pins 7 and 8 ($+V_{CC}$) remains within the 11.6V to 40V range as the output changes between the 4-20mA range (see Figure 4).
7. It is recommended that a reverse polarity protection diode (D_1 in Figure 1) be used. This will prevent damage to the XTR101 caused by a momentary (e.g., transient) or long term application of the wrong polarity of voltage between pins 7 and 8.

. Consider PC board layout which minimizes parasitic capacitance, especially in high gain.

ELECTING R_S

R_{SPAN} is chosen to that a given full scale input span e_{DIFS} will esult in the desired full scale output span of ΔI_{OFS}.

$$[(0.016Ʊ) + (40/R_S)]\ \Delta e_{IN} = \Delta I_O = 16\text{mA}.$$

olving for R_S:

$$R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016Ʊ} \qquad (1)$$

or example, if Δe_{INFS} = 100mV for ΔI_{OFS} = 16mA,

$$R_S = \frac{40}{16\text{mA}/100\text{mV}) - 0.016} = \frac{40}{0.16 - 0.016}$$

$$= \frac{40}{0.144} = 278\Omega$$

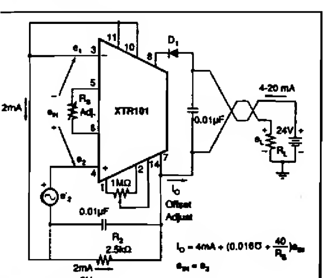
ee Typical Performance Curves for a plot of R_S vs Δe_{INFS}. Note that in order not to exceed the 20mA upper range limit, e_{IN} must be less than 1V when $R_S = \infty$ and proportionately maller as R_S decreases.

IASING THE INPUTS

ecause the XTR operates from a single supply both e_1 and e_2 must be biased approximately 5V above the voltage at pin to assure linear response. This is easily done by using one r both current sources and an external resistor R_2. Figure 5 hows the simplest case— a floating voltage source e'_2. The mA from the current sources flows through the 2.5kΩ alue of R_2 and both e_1 and e_2 are raised by the required 5V ith respect to pin 7. For linear operation the constraint is

$$+4\text{V} \le e_1 \le +6\text{V}$$
$$+4\text{V} \le e_2 \le +6\text{V}$$

he offset adjustment is used to remove the offset voltage of e input amplifier. When the input differential voltage (e_{IN}) juals zero, adjust for 4mA output.



GURE 5. Basic Connection for Floating Voltage Source.

Figure 6 shows a similar connection for a resistive transducer. The transducer could be excited either by one (as shown) or both current sources. Also, the offset adjustment has higher resolution compared to Figure 5.

CMV AND CMR

The XTR101 is designed to operate with a nominal 5V common-mode voltage at the input and will function properly with either input operating over the range of 4V to 6V with respect to pin 7. The error caused by the 5V CMV is already included in the accuracy specifications.

If the inputs are biased at some other CMV then an input offset error term is (CMV – 5)/CMRR; CMR is in dB, CMRR is in V/V.

SIGNAL SUPPRESSION AND ELEVATION

In some applications it is desired to have suppressed zero range (input signal elevation) or elevated zero range (input signal suppression). This is easily accomplished with the XTR101 by using the current sources to create the suppression/elevation voltage. The basic concept is shown in Figures 7 and 8(a). In this example the sensor voltage is derived from R_T (a thermistor, RTD, or other variable resistance element) excited by one of the 1mA current sources. The other current source is used to create the elevated zero range voltage. Figures 8(b), (c) and (d) show some of the possible circuit variations. These circuits have the desirable feature of noninteractive span and suppression/elevation adjustments. Note: It is not recommended to use the optional offset voltage null (pins 1, 2 and 14) for elevation/suppression. This trim capability is used only to null the amplifier's input offset voltage. In many applications the already low offset voltage (typically 20µV) will not need to be nulled at all. Adjusting the offset voltage to nonzero values will disturb the voltage drift by ±0.3µV/°C per 100µV or induced offset.

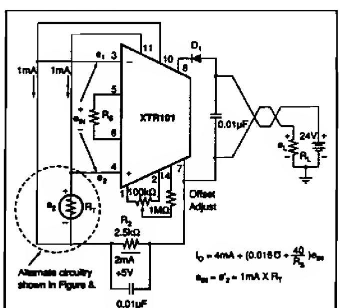


FIGURE 6. Basic Connection for Resistive Source.

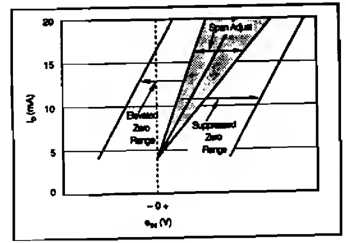


FIGURE 7. Elevation and Suppression Graph.

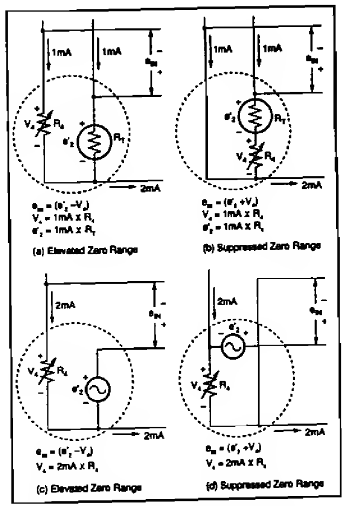


FIGURE 8. Elevation and Suppression Circuits.

APPLICATION INFORMATION

The small size, low offset voltage and drift, excellent linearity, and internal precision current sources, make the XTR101 ideal for a variety of two-wire transmitter applications. It can be used by OEMs producing different types of transducer transmitter modules and by data acquisition systems manufacturers who gather transducer data. Current mode transmission greatly reduces noise interference. The two-wire nature of the device allows economical signal conditioning at the transducer. Thus the XTR101 is, in general, very suitable for individualized and special purpose applications.

EXAMPLE 1

RTD Transducer shown in Figure 9.

Given a process with temperature limits of +25°C and +150°C, configure the XTR101 to measure the temperature with a platinum RTD which produces 100Ω at 0°C and 200Ω at +266°C (obtained from standard RTD tables). Transmit 4mA for +25°C and 20mA for +150°C.

COMPUTING R_S:

The sensitivity of the RTD is ΔR/ΔT = 100Ω/266°C. When excited with a 1mA current source for a 25°C to 150°C range (i.e., 125°C span), the span of e_{IN} is 1mA X (100Ω/266°C) X 125°C = 47mV = Δe_{IN}.

From equation 1, $R_S = \dfrac{40}{\Delta I_O/\Delta e_{IN} - 0.016\Omega}$

$$R_S = \frac{40}{16\text{mA}/47\text{mV} - 0.016Ʊ} = \frac{40}{0.3244} = 123.3\Omega$$

Span adjustment (calibration) is accomplished by trimming R_S.

COMPUTING R_4:

At +25°C, $e'_2 = 1\text{mA}\ (R_T + \Delta R_T)$

$$= 1\text{mA}\ [100\Omega + \frac{100\Omega}{266°\text{C}} \times 25°\text{C}]$$

$$= 1\text{mA}\ (109.4\Omega) = 109.4\text{mV}$$

In order to make the lower range limit of 25°C correspond to the output lower range limit of 4mA, the input circuitry shown in Figure 9 is used.

e_{IN}, the XTR101 differential input, is made 0 at 25°C or

$$e'_{2\,25°C} - V_4 = 0$$

$$\text{thus, } V_4 = e'_{2\,25°C} = 109.4\text{mV}$$

$$R_4 = \frac{V_4}{1\text{mA}} = \frac{109.4\text{mV}}{1\text{mA}} = 109.4\Omega$$

COMPUTING R_2 AND CHECKING CMV:

At +25°C, e'_2 = 109.4mV

At +150°C, $e'_2 = 1\text{mA}\ (R_T + \Delta R_T)$

$$= 1\text{mA}\ [100\Omega + (\frac{100\Omega}{266°\text{C}} \times 150°\text{C})]$$

$$= 156.4\text{mV}$$

Since both e'_2 and V_4 are small relative to the desired 5V common-mode voltage, they may be ignored in computing R_2 as long as the CMV is met.

R_2 = 5V/2mA = 2.5kΩ

e_2 min = 5V + 0.1094V
e_2 max = 5V + 0.1564V
e_1 = 5V + 0.1094V

The +4V to +6V CMV requirement is met.

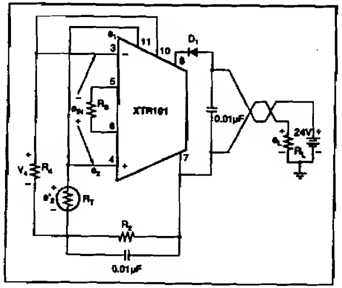


FIGURE 9. Circuit for Example 1.

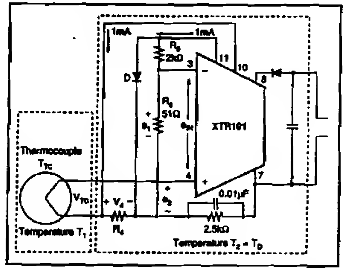


FIGURE 10. Thermocouple Input Circuit with Two Temperature Regions and Diode (D) Cold Junction Compensation.

EXAMPLE 2

Thermocouple Transducer shown in Figure 10.

Given a process with temperature (T_1) limits of 0°C and +1000°C, configure the XTR101 to measure the temperature with a type J thermocouple that produces a 58mV change for 1000°C change. Use a semiconductor diode for a cold junction compensation to make the measurement relative to 0°C. This is accomplished by supplying a compensating voltage, V_{R6}, equal to that normally produced by the thermocouple with its "cold junction" (T_2) at ambient. At a typical ambient of +25°C this is 1.28mV (obtained from standard thermocouple tables with reference junction of 0°C). Transmit 4mA for T_1 = 0°C and 20mA for T_1 = +1000°C. Note: $e_{IN} = e_2 - e_1$ indicates that T_1 is relative to T_2.

ESTABLISHING R_S:

The input full scale span is 58mV (Δe_{INFS} = 58mV).

R_S is found from equation (1)

$$R_S = \frac{40}{\Delta I_O/\Delta e_{IN} - 0.016\mho}$$

$$= \frac{40}{16mA/58mV - 0.016\mho} = \frac{40}{0.2599} = 153.9\Omega$$

SELECTING R_4:

R_4 is chosen to make the output 4mA at T_{TC} = 0°C (V_{TC}= –1.28mV) and T_D = +25°C (V_D = 0.6V). A circuit is shown in Figure 10.

V_{TC} will be –1.28mV when T_{TC} = 0°C and the reference junction is at +25°C. e_1 must be computed for the condition of T_D = +25°C to make e_{IN} = 0V.

$$V_{D\,25°C} = 600mV$$

$$e_{1\,25°C} = 600mV\ (51/2051) = 14.9mV$$

$$e_{IN} = e_2 - e_1 = V_{TC} + V_4 - e_1$$

With e_{IN} = 0 and V_{TC} = –1.28mV,

$$V_4 = e_1 + e_{IN} - V_{TC}$$

$$= 14.9mV + 0V - (-1.28mV)$$

$$1mA\ (R_4) = 16.18mV$$

$$R_4 = 16.18\Omega$$

COLD JUNCTION COMPENSATION:

The temperature reference circuit is shown in Figure 11.

The diode voltage has the form

$$V_D = \frac{KT}{q} \ln \frac{I_{DIODE}}{I_{SAT}}$$

Typically at T_2 = +25°C, V_D = 0.6V and $\Delta V_D/\Delta T$ = –2mV/°C. R_5 and R_6 form a voltage divider for the diode voltage V_D. The divider values are selected so that the gradient $\Delta_V D/\Delta T$ equals the gradient of the thermocouple at the reference temperature. At +25°C this is approximately 52µV/°C (obtained from standard thermocouple table); therefore,

$$\Delta T_C/\Delta T = \Delta_V D/\Delta T \left[\frac{R_6}{R_5 + R_6}\right] \quad (2)$$

$$52\mu V/°C = 2000\mu V/°C \left[\frac{R_6}{R_5 + R_6}\right]$$

R_5 is chosen as 2kΩ to be much larger than the resistance of the diode. Solving for R_6 yields 51Ω.

THERMOCOUPLE BURN-OUT INDICATION

In process control applications it is desirable to detect when a thermocouple has burned out. This is typically done by forcing the two-wire transmitter current to either limit when

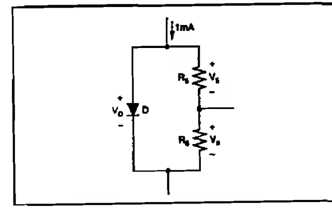


FIGURE 11. Cold Junction Compensation Circuit.

the thermocouple impedance goes very high. The circuits of Figures 16 and 17 inherently have down scale indication. When the impedance of the thermocouple gets very large (open) the bias current flowing into the + input (large impedance) will cause I_O to go to its lower range limit value (about 3.8mA). If up scale indication is desired the circuit of Figure 18 should be used. When the T_C opens the output will go to its upper range limit value (about 25mA or higher).

OPTIONAL INPUT OFFSET VOLTAGE TRIM

The XTR101 has provisions for nulling the input offset voltage associated with the input amplifiers. In many applications the already low offset voltages (30µV max for the B grade, 60µV max for the A grade) will not need to be nulled at all. The null adjustment can be done with a potentiometer at pins 1, 2 and 14 as shown in Figures 5 and 6. Either of these two circuits may be used. NOTE: It is not recommended to use this input offset voltage nulling capability for elevation or suppression. See the Signal Suppression and Elevation section for the proper techniques.

OPTIONAL BANDWIDTH CONTROL

Low-pass filtering is recommended where possible and can be done by either one of two techniques shown in Figure 12. C_2 connected to pins 3 and 4 will reduce the bandwidth with a cutoff frequency given by,

$$f_{CO} = \frac{15.9}{(R_1 + R_2 + R_3 + R_4)\ (C_2 + 3pF)}$$

This method has the disadvantage of having f_{CO} vary with R_1, R_2, R_3, R_4, and it may require large values of R_3 and R_4. The other method, using C_1, will use smaller values of capacitance and is not a function of the input resistors. It is, however, more subject to nonlinear distortion caused by slew rate limiting. This is normally not a problem with the slow signals associated with most process control transducers. The relationship between C_1 and f_{CO} is shown in the Typical Performance Curves.

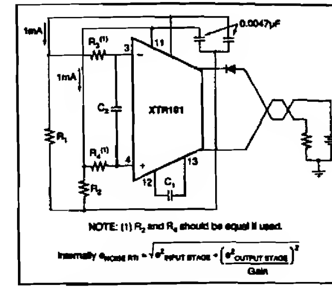


FIGURE 12. Optional Filtering.

APPLICATION CIRCUITS

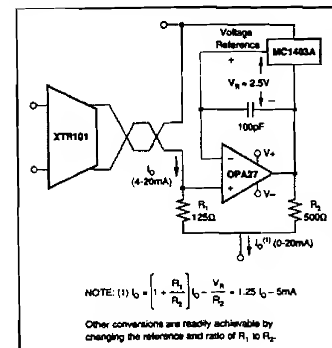


FIGURE 13. 0-20mA Output Converter.

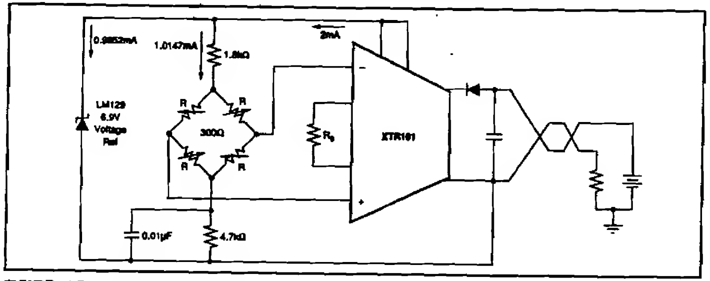


FIGURE 14. Bridge Input, Voltage Excitation.

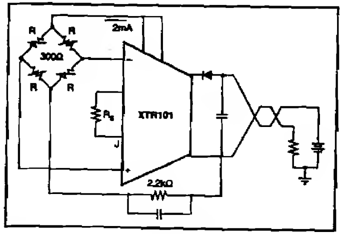


FIGURE 15. Bridge Input, Current Excitation.

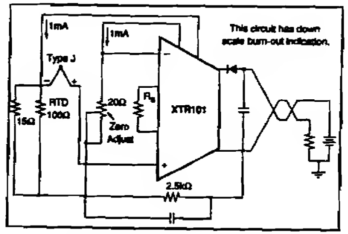


FIGURE 16. Thermocouple Input with RTD Cold Junction Compensation.

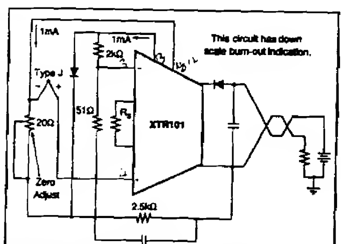


FIGURE 17. Thermocouple Input with Diode Cold Junction Compensation.

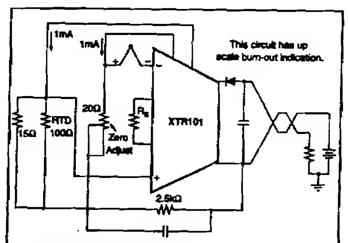


FIGURE 18. Thermocouple Input with RTD Cold Junction Compensation.

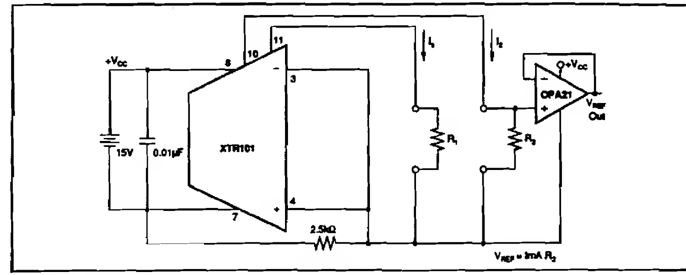


FIGURE 19. Dual Precision Current Sources Operated From One Supply.

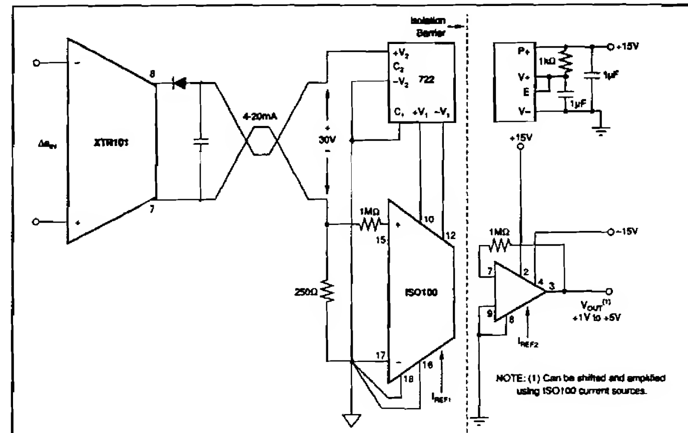


FIGURE 20. Isolated Two-Wire Current Loop.

DETAILED ERROR ANALYSIS

The ideal output current is

$$i_{O\ IDEAL} = 4mA + K\ e_{IN}$$

K is the span (gain) term, $(0.016\Omega + (40/R_S))$ (3)

In the XTR101 there are three major components of error:

1. σ_O = errors associated with the output stage.
2. σ_S = errors associated with span adjustment.
3. σ_I = errors associated with the input stage.

The transfer function including these errors is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K(1 + \sigma_S)(e_{IN} + \sigma_I) \quad (4)$$

When this expression is expanded, second order terms $(\sigma_S\ \sigma_I)$ dropped, and terms collected, the result is

$$i_{O\ ACTUAL} = (4mA + \sigma_O) + K\ e_{IN} + K\sigma_I + K\sigma_S\ e_{IN} \quad (5)$$

The error in the output current is $i_{O\ ACTUAL} - i_{O\ IDEAL}$ and can be found by subtracting equations (5) and (3).

$$i_{O\ ERROR} = \sigma_O + K\sigma_I + K\sigma_S\ e_{IN} \quad (6)$$

This is a general error expression. The composition of each component of error depends on the circuitry inside the XTR101 and the particular circuit in which it is applied. The circuit of Figure 9 will be used to illustrate the principles.

1. $\sigma_O = I_{OS\ RTO}$ (7)
2. $\sigma_S = \varepsilon_{NONLINEARITY} + \varepsilon_{SPAN}$ (8)
3. $\sigma_I = V_{OSI} + (I_{B1} + R_4 - I_{B2}\ R_T) + \dfrac{\Delta V_{CC}}{PSRR} + \dfrac{(e_1 + e_2)/2 - 5V}{CMRR}$ (9)

The term in parentheses may be written in terms of offset current and resistor mismatches as $I_{B1}\ \Delta R + I_{OS}'\ R_4$.

- V_{OSI}* = input offset voltage
- I_{B1}*, I_{B2}* = input bias current
- I_{OSI}* = input offset current
- $I_{OS\ RTO}$* = output offset current error
- ΔR = $R_T - R_4$ = mismatch in resistor
- ΔV_{CC} = change supply voltage between pins 7 and 8 away from 24V nominal
- PSRR* = power supply rejection ratio
- CMRR* = common-mode rejection ratio
- ε_{NONLIN}* = span nonlinearity
- ε_{SPAN}* = span equation error. Untrimmed error = 5% max. May be trimmed to zero.

Items marked with an asterisk (*) can be found in the Electrical Specifications.

EXAMPLE 3

The circuit in Figure 9 with the XTR101BG specifications and the following conditions: $R_T = 109.4\Omega$ at 25°C, $R_T = 156.4\Omega$ at 150°C, $I_O = 4mA$ at 25°C, $I_O = 20mA$ at 150°C, $R_S = 123.3\Omega$, $R_4 = 109\Omega$, $R_L = 250\Omega$, $R_{LINE} = 100\Omega$, $V_{DI} = 0.6V$, $V_{PS} = 24V \pm 0.5\%$. Determine the % error at the upper and lower range values.

A. AT THE LOWER RANGE VALUE (T = +25°C).

$$\sigma_O = I_{OS\ RTO} = \pm 6\mu A$$

$$\sigma_I = V_{OSI} + (I_{B1}\ \Delta R + I_{OSI}\ R_4) + \frac{\Delta V_{CC}}{PSRR} + \frac{(e_1 + e_2)/2 - 5V}{CMRR}$$

$$\Delta R = R_{T\ 25°C} - R_4 = 109.4 - 109 \approx 0$$

$$\Delta V_{CC} = (24 \times 0.005) + 4mA\ (250\Omega + 100\Omega) + 0.6V = 120mV + 1400mV + 600mV = 2120mV$$

$$e_1 = (2mA \times 2.5k\Omega) + (1mA \times 109\Omega) = 5.109V$$
$$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 109.4\Omega) = 5.1094V$$

$$(e_1 + e_2)/2 - 5 = 0.1092V$$

PSRR = 3.16×10^5 for 110dB

CMRR = 31.6×10^3 for 90dB

$$\sigma_I = 30\mu V + (150nA \times 0 + 20nA \times 109\Omega) + \frac{2120mV}{3.16 \times 10^5} + \frac{0.1092V}{3.16 \times 10^3} \quad (10)$$

$$= 30\mu V + 2.18\mu V + 6.7\mu V + 3.46\mu V = 42.34\mu V$$

$$\sigma_S = \varepsilon_{NONLIN} + \varepsilon_{SPAN} = 0.0001 + 0 \text{ (assumes trim of } R_S)$$

$$I_O \text{ error} = \sigma_O + K\ \sigma_I + K\ \sigma_S\ e_{IN}$$

$$K = 0.016 + \frac{40}{R_S} = 0.016 + \frac{40}{123.3\Omega} = 0.340\mho$$

$$e_{IN} = e_2 - V_4 = I_{REF1}\ R_{T\ 25°C} - I_{REF2}\ R_4$$

since $R_{T\ 25°C} = R_4$,

$$e_{IN} = (I_{REF1} - I_{REF2})\ R_4 = 0.4\mu A \times 109\Omega \approx 43.6\mu V$$

Since the maximum mismatch of the current references is 0.04% of 1mA = 0.4µA,

$$I_O \text{ error} = 6\mu A + (0.34\mho \times 42.34\mu V) + (0.34\mho \times 0.0001 \times 43.6\mu V) = 6\mu A + 14.40\mu A + 0.0015\mu A = 20.40\mu A$$

$$\% \text{ error} = \frac{20.40\mu A}{16mA} \times 100\%$$

0.13% of span at lower range value.

B. AT THE UPPER RANGE VALUE (T = +150°C).

$$\Delta R = R_{T\ 150°C} - R_4 = 156.4 - 109.4 = 47\Omega$$

$$\Delta V_{CC} = (24 \times 0.005) + 20mA\ (250\Omega + 100\Omega) + 0.6V = 7720mV$$

$$e_1 = 5.109V$$

$$e_2 = (2mA \times 2.5k\Omega) + (1mA \times 156.4\Omega) = 5.156V$$

$$(e_1 + e_2)/2 - 5V = 0.1325V$$

$$\sigma_O = 6\mu A$$

$$\sigma_I = 30\mu V + (150nA \times 47\Omega + 20nA \times 190\Omega) + \frac{7720mV}{3.16 \times 10^5} + \frac{0.1325V}{3.16 \times 10^3}$$

$$= 30\mu V + 9.23\mu V + 24\mu V + 4.19\mu V = 67.42\mu V$$

$$\sigma_S = 0.0001$$

$$e_{IN} = e'_2 - V_4 = I_{REF1}\ R_{T\ 150°C} - I_{REF2}\ R_4 = (1mA \times 156.4\Omega) - (1mA \times 109\Omega) = 47mV$$

$$I_O \text{ error} = \sigma_O + K\ \sigma_I + K\ \sigma_S\ e_{IN} = 6\mu A + (0.34\mho \times 67.42\mu V) + (0.34\mho \times 0.0001 \times 47000\mu V) = 6\mu A + 22.92\mu A + 1.60\mu A = 30.52\mu A$$

$$\% \text{ error} = \frac{30.52\mu A}{16mA} \times 100\%$$

= 0.19% of span at upper range value.

CONCLUSIONS

Lower Range: From equation (10) it is observed that the predominant error term is the input offset voltage (30µV for the B grade). This is of little consequence in many applications. $V_{OS\ RTI}$ can, however, be nulled using the pot shown in Figures 5 and 6. The result is an error of 0.06% of span instead of 0.13% if span.

Upper Range: From equation (11), the predominant errors are $I_{OS\ RTO}$ (6µA), $V_{OS\ RTI}$ (30µV), and I_B (150nA), max, B grade. Both I_{OS} and V_{OS} can be trimmed to zero; however, the result is an error of 0.09% of span instead of 0.19% span.

RECOMMENDED HANDLING PROCEDURES FOR INTEGRATED CIRCUITS

All semiconductor devices are vulnerable, in varying degrees, to damage from the discharge of electrostatic energy. Such damage can cause performance degradation or failure, either immediate or latent. As a general practice, we recommend the following handling procedures to reduce the risk of electrostatic damage.

1. Remove the static-generating materials, such as untreated plastic, from all areas that handle microcircuits.
2. Ground all operators, equipment, and work stations.
3. Transport and ship microcircuits, or products incorporating microcircuits, in static-free, shielded containers.
4. Connect together all leads of each device by means of a conductive material, when the device is not connected into a circuit.
5. Control relative humidity to as high a value as practical (50% recommended).